Coplanar Waveguides for MMIC Applications: Effect of Upper Shielding, Conductor Backing, Finite-Extent Ground Planes, and Line-to-Line Coupling

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Abstract —Parasitic effects occurring in actual realizations of coplanar waveguides (CPW) for microwave integrated circuits on GaAs substrates, such as the influence of an upper shield, conductor backing, finite-extent ground planes, and line-to-line coupling, are discussed and evaluated. CAD-oriented analytical expressions are obtained for the electrical quasi-TEM parameters of the relevant waveguiding structures by means of exact or approximate conformal mapping techniques. Differences in electrical behavior with respect to ideal CPW's are highlighted, and practical design criteria are obtained for keeping cover height, ground-plane width, and line-to-line spacing effects to a minimum.

I. Introduction

Coplanar waveguides (CPW's) offer several advantages over conventional microstrips for monolithic or hybrid microwave integrated circuits (MIC) applications on GaAs substrates [1]; these include ease of parallel and series insertion of both active and passive components and high circuit density. However, their use in actual circuit design has been somehow less widespread than would have been expected. This is due not only to incidental reasons, such as a comparative lack of experience and CAD facilities in coplanar circuit design, but also to intrinsic difficulties encountered whenever coplanar lines are used in circuits having complex layouts. In fact, the fields of CPW's are less confined than those of microstrip lines, thereby increasing their sensitivity to environmental constraints, such as upper shielding, conductor backing, lateral ground plane truncation, and line-to-line coupling. Among these, upper shielding is almost always present in monolithic MIC's (MMIC's), whereas lateral shielding by means of grounded vertical electric planes is not common, and therefore will not be considered here. Moreover, a parasitic form of shielding occurs in hybrid or microhybrid circuits when flip-chip active elements are inserted. Conductor backing is often introduced in order to improve both the mechanical strength and the power-handling capability of the line [2]–[4]; moreover, it allows easy implementation of mixed coplanar–microstrip circuits. Both shielding and conductor backing lower the impedance level of the line. A further difference between ideal CPW's and actual implementations is the fact that the lateral ground planes of actual CPW's have finite width. The ground-plane width should be as small as possible, since it has a direct influence upon the maximum line density achievable in coplanar circuits. Truncating the lateral ground planes causes the impedance of the line to become higher and increases line-to-line coupling. Moreover, a CPW with finite ground planes supports a quasi-TEM slotlike mode whose impedance level can be comparable to the one of the desired even mode. This mode can be strongly excited in correspondence of discontinuities and external transitions with other lines if the lateral ground planes are not kept at the same (ground) potential by means of properly spaced conductive bridges. Complex circuit topologies often lead to areas of metallization which should theoretically be grounded but are actually floating. Since grounding cannot be easily achieved by means of via holes, as in microstrip circuits, conductor backing represents a possible solution to this problem. Finally, coupling effects between conductor pairs must be accounted for and possibly avoided in circuits with high line density. On the other hand, the spacing between lines should not be unnecessarily large, since this would amount to increasing the circuit size. A tradeoff between these two constraints can be suggested by a quantitative estimate of line-to-line coupling.

In the present paper, parasitic effects occurring when coplanar lines are conductor backed or shielded, or both, are discussed in detail and evaluated from a quantitative point of view. The influence of the finite extent of lateral ground planes on the impedance level of the line is also dealt with. The propagation characteristics of the odd mode supported by a CPW with finite ground planes are investigated in order to give better insight into whether this mode can be excited in the case of poor grounding. Finally, line-to-line coupling between CPW's is discussed and evaluated.

Simple analytical formulas for the quasi-TEM parameters obtained from either exact or approximate conformal mapping techniques are proposed, accounting for the aforementioned effects, and results are presented relevant

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to MIC's on GaAs substrates ($\epsilon_r = 13.0$) with the aim of providing design criteria for shield spacings, ground-plane widths, and line-to-line spacings; alternatively, the design formulas provided can be used in order to exploit the flexibility provided by additional parameters such as the lateral ground-plane width or the cover height.

It is well known that the quasi-static analysis is rigorously valid only at zero frequency. Therefore, it may be questionable whether this analysis yields reasonably accurate results beyond the C-band or, still less, the X-band. However, it should be taken into account that in MIC applications, both substrate thickness and line dimensions are reduced with respect to microstrip lines on conventional substrates. The frequency range whereon the quasi-static approach gives fairly accurate results is therefore expected to extend well beyond the X-band. Although making quantitative estimates on this point may be difficult, owing to the lack of closed-form expressions for the frequency-dependent parameters of coplanar lines, some general conclusions can be drawn from numerical data published in the literature, for instance from the results shown in [4]. From [4, Fig. 2(a)], one sees that for conductor-backed CPW's on a GaAs substrate with a thickness h of 150 μm and a strip width of 100 μm, dispersion is negligible in the range 0–40 GHz. By rescaling all dimensions and taking into account that 200 μm is a somewhat large value for the strip width, the useful range of the quasi-TEM approximation is expected to extend well beyond 20 GHz for a substrate thickness h of 300 μm. Realistic substrate thicknesses for MIC's usually lie in the range 100–300 μm. While conductor-backed CPW's are remarkably less dispersive than microstrips, at least for slot widths not larger than the substrate thickness, free-standing CPW's show the same degree of dispersivity as microstrips. Nevertheless, even in the latter case, the actual amount of dispersion is rather small for MIC lines (see [4, Fig. 2(b)]); for instance, the phase velocity relative variation for a CPW on an infinitely thick GaAs substrate having a strip width of 200 μm and a slot width of 100 μm (which can be considered as fairly large values for MMIC's) amounts to only 2 percent in the range 0–40 GHz. Therefore, as a general conclusion, one can expect the quasi-TEM approximation to yield meaningful results in the frequency band whereon MIC's usually operate today, at least for those structures and components which are not particularly frequency-sensitive.

II. Analysis of the Relevant Waveguiding Structures

Four waveguiding structures will be considered in order to analyze the effects discussed in the Introduction: the coplanar waveguide with upper shielding (Fig. 1(a)), the conductor-backed coplanar waveguide with upper shielding (Fig. 1(b)), and the coplanar waveguide with finite-extent ground planes excited both in the even and in the odd (parasitic) mode (Fig. 1(c)). For the sake of brevity, these structures will be referred to in what follows as CPW1, CPW2, CPW3, and CPW4, respectively. Finally, the coupling between two CPW's on an infinitely thick substrate is considered (Fig. 1(d)).

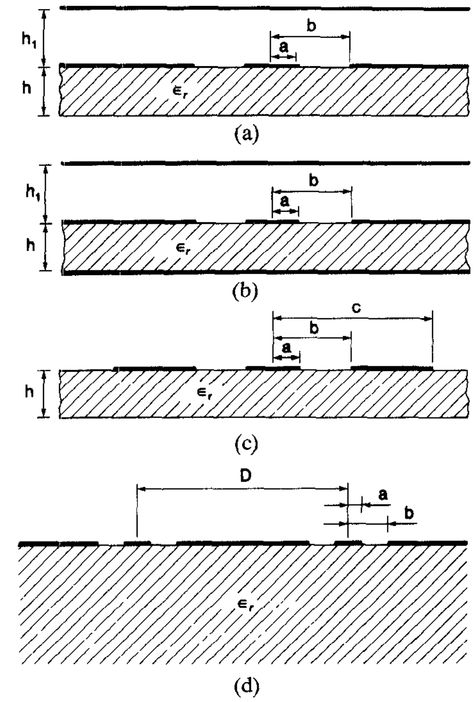

Fig. 1. (a) Coplanar waveguide with upper shielding (CPW1). (b) Conductor-backed coplanar waveguide with upper shielding (CPW2). (c) Coplanar waveguide with finite lateral ground planes (CPW3, even mode; CPW4, odd mode). (d) Coupled parallel coplanar waveguides.

A. Coplanar Waveguide With Upper Shielding

Analytical expressions for the quasi-TEM electrical parameters (characteristic impedance Z_1 and effective permittivity ϵ_{eff1}) of CPW1 (Fig. 1(a)) can be obtained if the two slots are modeled as magnetic walls. Although this assumption is hardly verified for large slots and very small cover heights, it has proven to yield excellent results for practical line dimensions [3]. Thus, the overall capacitance per unit length of the line can be computed as the sum of the capacitance of the upper half-plane (in air) and lower half-plane (air and dielectric layer). The latter capacitance can be evaluated by means of the approximate technique first suggested in [6] (see also [5]) as the sum of the free-space capacitance in the absence of the dielectric and the capacitance of the dielectric layer, assumed to have permittivity $\epsilon_r - 1$. In other words, the second contribution is obtained by replacing all air–dielectric interfaces by magnetic walls and the dielectric substrate by an equivalent dielectric of permittivity $\epsilon_r - 1$. It ought to be noted that this technique yields exact results both for infinitely thick substrates and for $h \to 0$. The capacitance of the upper half-plane is computed exactly through the sequence of conformal mappings outlined in Fig. 2. First, the dashed region within the upper right quadrant (Fig. 2(a)) is mapped onto the upper t half-plane (Fig. 2(b)) by means of the transformation

$$t = \cosh^2(\pi x / 2h_1) \tag{1}$$

and then onto the rectangular domain of Fig. 2(c) through

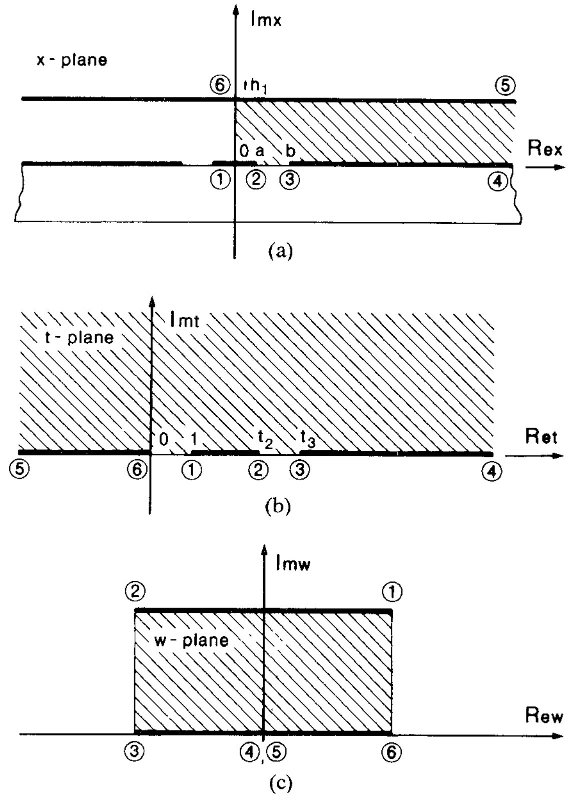

Fig. 2. Conformal mapping for CPW1: (a) original structure; (b) intermediate t-plane; (c) final mapping into a plane-parallel capacitor. The transformed region is dashed.

the mapping

$$w=\int_{t_0}^{t}\frac{dt}{\sqrt{t(t-1)(t-t_1)(t-t_2)}}. \tag{2}$$

Let us call the resulting quarter-plane capacitance C_{11}; if the total capacitance of the lower half-plane is referred to as C_{12}, the overall capacitance per unit length of the line is

$$\begin{aligned}C_1(\epsilon_r)&=2C_{11}+C_{12}\\&=2\epsilon_0\frac{K(k_2)}{K(k_2')}+2\epsilon_0\frac{K(k)}{K(k')}+2(\epsilon_r-1)\epsilon_0\frac{K(k_1)}{K(k_1')}\end{aligned} \tag{3}$$

where

$$k=a/b \tag{4a}$$

$$k_1=\sinh(\pi a/2h)/\sinh(\pi b/2h) \tag{4b}$$

$$k_2=\tanh(\pi a/2h_1)/\tanh(\pi b/2h_1). \tag{4c}$$

$K(k)$ is the complete elliptic integral of the first kind, and $k_i'=\sqrt{(1-k_i^2)}$. Therefore, the effective permittivity and characteristic impedance are, respectively,

$$\epsilon_{\text{eff}1}=\frac{C_2(\epsilon_r)}{C_1(1)}=1+q_1(\epsilon_r-1) \tag{5a}$$

where the filling factor q_1 is expressed as

$$q_1=\frac{\dfrac{K(k_1)}{K(k_1')}}{\dfrac{K(k_2)}{K(k_2')}+\dfrac{K(k)}{K(k')}} \tag{5b}$$

and

$$Z_{01}=\frac{60\pi}{\sqrt{\epsilon_{\text{eff}1}}}\frac{1}{\dfrac{K(k_2)}{K(k_2')}+\dfrac{K(k)}{K(k')}}. \tag{6}$$

B. Conductor-Backed Coplanar Waveguide With Upper Shielding

For the second waveguiding structure considered (CPW2, Fig. 1(b)), the capacitance per unit length is obtained by making use of the transformation already introduced to map the upper half of CPW1 into a rectangle. Once again, the two slots are modeled as magnetic walls; this assumption is rigorously correct only if $h=h_1$, but it leads to excellent results for practical structures. It should be borne in mind that, in practical circuits, conductor-backed CPW's are never designed in order to have prevailing microstrip behavior (occurring for wide central conductor or large slots), lest the advantages of small size permitted by ideal CPW's be nullified. The resulting capacitance per unit length is

$$C_2(\epsilon_r)=2\epsilon_0\epsilon_r\frac{K(k_3)}{K(k_3')}+2\epsilon_0\frac{K(k_4)}{K(k_4')} \tag{7}$$

where

$$k_3=\tanh(\pi a/2h)/\tanh(\pi b/2h) \tag{8a}$$

$$k_4=\tanh(\pi a/2h_1)/\tanh(\pi b/2h_1). \tag{8b}$$

For the effective permittivity and characteristic impedance, one has

$$\epsilon_{\text{eff}2}=\frac{C_2(\epsilon_r)}{C_2(1)}=1+q_2(\epsilon_r-1) \tag{9a}$$

with filling factor q_2:

$$q_2=\frac{\dfrac{K(k_3)}{K(k_3')}}{\dfrac{K(k_3)}{K(k_3')}+\dfrac{K(k_4)}{K(k_4')}} \tag{9b}$$

and

$$Z_{02}=\frac{60\pi}{\sqrt{\epsilon_{\text{eff}2}}}\frac{1}{\dfrac{K(k_3)}{K(k_3')}+\dfrac{K(k_4)}{K(k_4')}}. \tag{10}$$

In order to validate the approximations made in obtaining formulas (9) and (10), the related results are compared (Fig. 3) with the electrical parameters computed by solving the Laplace equation in the transversal domain by means of standard finite-element (FEM) technique [7]. The actual structure analyzed with FEM is also laterally shielded, but the lateral ground planes have been removed far enough to make their influence on the line parameters negligible. One should note that if $h_1=h$ ($h/b=1$ curve), conformal mapping yields exact results and the effective permittivity is $\epsilon_{\text{eff}2}=(\epsilon_r+1)/2$. If the cover height h_1 tends to infinity, $k_4\to a/b$ and the simple conductor-backed coplanar

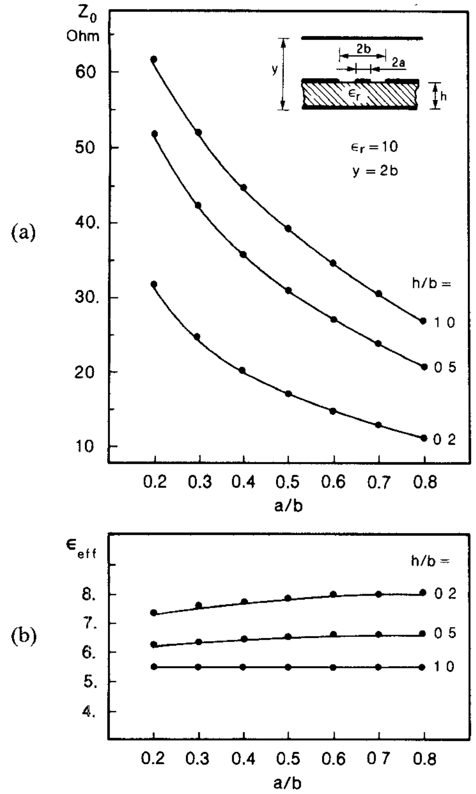

Fig. 3. Conductor-backed coplanar waveguides with upper shield: comparison between the electrical parameters computed numerically (continuous lines) and the present results (dots). (a) Impedance and (b) effective permittivity as a function of the shape ratio a/b and substrate thickness h/b.

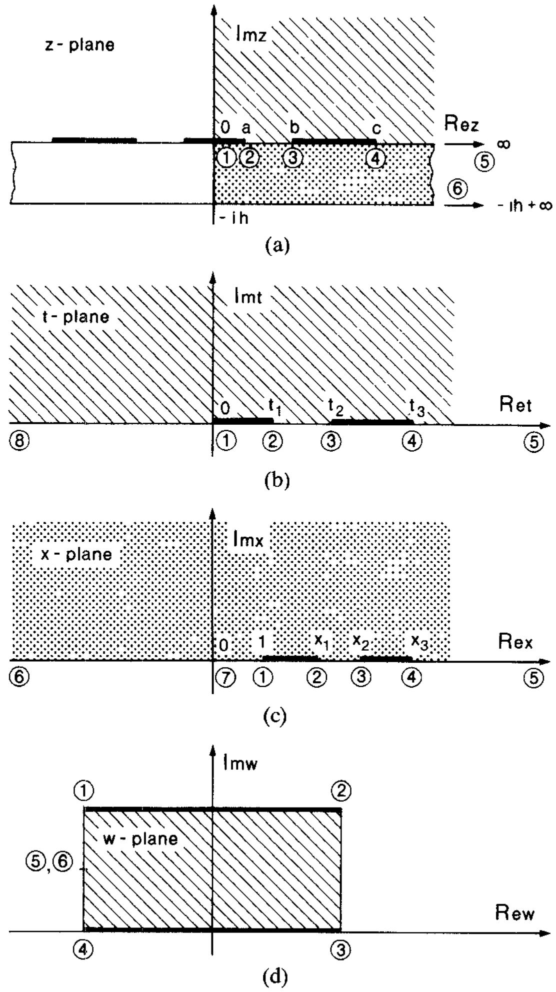

Fig. 4. Conformal mapping for CPW2: (a) original structure; (b) intermediate transformed plane for the dashed region; (c) intermediate transformed plane for the dotted region; (d) final mapping into a plane-parallel capacitor (valid for both regions).

waveguide already discussed in [3] is obtained. This last line shows a marked impedance reduction with respect to the free-standing line, unless the substrate is very thick.

C. Coplanar Waveguide With Finite-Extent Ground Planes: Even Mode

The parameters of a coplanar waveguide having finite-extent lateral ground planes (CPW3, Fig. 1(c), even mode) can be computed by following the sequence of conformal mappings shown in Fig. 4(a)–(d). According to the formulation of [5] and [6], the overall capacitance per unit length of the line is approximated again by summing the free-space capacitance and the capacitance of a line where the field is confined in the dielectric layer, assumed to be of permittivity $\epsilon_r - 1$. As far as the first contribution is concerned, the first quadrant of Fig. 4(a) is transformed into the upper t half-plane of Fig. 4(b) by the mapping $t = z^2$ and then into the rectangular region of Fig. 4(d) through the mapping

$$w = \int_{t_0}^{t} \frac{dt}{\sqrt{t(t-1)(t-t_1)(t-t_2)}}. \tag{11}$$

The air capacitance per unit length is therefore

$$C_{31} = 4\epsilon_0 \frac{\overline{12}}{\overline{23}} = 4\epsilon_0 \frac{K(k_5)}{K(k_5')} \tag{12}$$

$$k_5 = \frac{a}{b}\sqrt{\frac{1-b^2/c^2}{1-a^2/c^2}} \tag{13}$$

where $\overline{ij}$ is the distance between points i and j in the w plane. In order to compute the second capacitance contribution, the dielectric–air interfaces are replaced by magnetic walls, and the permittivity is set to $\epsilon_r - 1$. The region corresponding to the dielectric layer in Fig. 4(a) is transformed into the lower x half-plane (Fig. 4(c)) by means of the mapping $x = \cosh^2(\pi z/2h)$ and then into the rectangular domain of Fig. 4(d) via the mapping

$$w = \int_{x_0}^{x} \frac{dx}{\sqrt{(x-1)(x-x_1)(x-x_2)(x-x_3)}}. \tag{14}$$

The layer capacitance is therefore

$$C_{32} = 2\epsilon_0 \frac{\overline{12}}{\overline{23}} = 2\epsilon_0(\epsilon_r - 1)\frac{K(k_6)}{K(k_6')} \tag{15}$$

$$k_6 = \frac{\sinh(\pi a/2h)}{\sinh(\pi b/2h)}\sqrt{\frac{1-\sinh^2(\pi b/2h)/\sinh^2(\pi c/2h)}{1-\sinh^2(\pi a/2h)/\sinh^2(\pi c/2h)}} \tag{16}$$

and the overall capacitance per unit length of the line can be expressed as $C_3 = C_{31} + C_{32}$. Thus, the effective permittivity and characteristic impedance take on the expressions

$$\epsilon_{\mathrm{eff}\,3} = \frac{C_3(\epsilon_r)}{C_3(1)} = 1 + q_3(\epsilon_r - 1) \tag{17a}$$

with filling factor q_3:

$$q_3 = \frac{1}{2} \frac{K(k_6)}{K(k_6')} \frac{K(k_5')}{K(k_5)} \tag{17b}$$

and

$$Z_{03} = \frac{30\pi}{\sqrt{\epsilon_{\mathrm{eff}\,3}}} \frac{K(k_5')}{K(k_5)}. \tag{18}$$

D. Coplanar Waveguide With Finite-Extent Ground Planes: Odd Parasitic Mode

For the last structure (CPW4, Fig. 1(c), odd mode), only the final result will be given, for the sake of brevity. For the scope of evaluating the effects discussed in the present paper, we shall limit ourselves to the case where the substrate is infinitely thick. In this case, one obtains for the line parameters the following exact results:

$$\epsilon_{\mathrm{eff}\,4} = \frac{\epsilon_r + 1}{2} \tag{19}$$

$$Z_{04} = \frac{120\pi}{\sqrt{\epsilon_{\mathrm{eff}\,4}}} \frac{K(k_7)}{K(k_7')} \tag{20}$$

where

$$k_7 = \frac{b}{c}\sqrt{\frac{1 - a^2/b^2}{1 - a^2/c^2}}. \tag{21}$$

The odd-mode impedance is normalized so that Z_{04} tends to the impedance of a coplanar stripline (CPS, see [5]) for $a \to 0$. On the other hand, the even-mode impedance is normalized so that Z_{03} yields, for $c \to \infty$, the impedance of an ordinary CPW. This is not the customary normalization for even–odd impedance pairs, based upon the even–odd-mode capacitances to ground. According to this normalization, one should take as the even-mode impedance $2Z_{03}$ and as the odd-mode impedance $Z_{04}/2$. For $c \to \infty$, the characteristic impedance of the odd mode goes to zero; in other words, this mode does not exist if the ground planes have infinite extent. In spite of this fact, for practical lateral ground plane widths, the mode can have a high impedance level. Note that finite-thickness substrates lead to an increase of the characteristic impedance. Thus, the impedance levels of both modes (even and odd) turn out to be comparable.

E. Coupling Between Parallel Coplanar Lines

Let us consider the structure of Fig. 1(d). Since we are interested in a rough estimate of the coupling between the two CPW's for the case where the coupling is very low, we neglect the effects due to finite substrate. At any rate, this leads to a conservative estimate for the minimum line-to-line spacing, since an infinitely thick substrate increases coupling. As is well known, the coupling factor between the two lines can be expressed as

$$C = -20\log_{10}\frac{Z_e - Z_o}{Z_e + Z_o} \tag{22}$$

where Z_e and Z_o are the even- and odd-mode impedances, respectively, of the structure of Fig. 1(d) considered as a two-conductor coupler. The exact evaluation of C is rather cumbersome; however, suitable approximations can be made if the coupling is low, which is indeed the case under examination. For low coupling, one has $Z_e = Z_\infty + \Delta Z_e$, $Z_o = Z_\infty - \Delta Z_o$, where Z_∞ is the line impedance when the spacing D becomes infinite, and ΔZ_e, $\Delta Z_o \ll Z_\infty$. Moreover, the odd-mode impedance is more sensitive to spacing than the even-mode; therefore, one certainly has $\Delta Z_o > \Delta Z_e$. Finally, for very low coupling, $\Delta Z_e \sim \Delta Z_o$. If we set $\Delta Z_e \approx \Delta Z_o$, the coupling C is slightly overestimated, but, even in the worst case, in which $\Delta Z_e = 0$, the maximum error amounts to 6 dB. Since coupling can be considered negligible for values ranging from -30 to -50 dB, such error is small enough. The parameter ΔZ_o can be evaluated exactly by means of conformal mapping; the resulting approximate coupling coefficient takes on the simple expression

$$C = -20\log_{10}(1 - Z_o/Z_\infty) \tag{23}$$

where

$$\frac{Z_o}{Z_\infty} = \frac{K(k_8')}{K(k_8)} \frac{K(k_9)}{K(k_9')} \tag{24}$$

$$k_9 = \frac{2\sqrt{ab}}{a+b} \tag{25a}$$

$$k_8 = \frac{k_9}{\left[1 - (b-a)^2/D^2\right]^{1/2}}. \tag{25b}$$

Note that k_9 is the limit of k_8 for $D \to \infty$ (uncoupled lines).

III. Results and Design Criteria

In this section, some results concerning lines on GaAs substrates will be given, with the aim of suggesting practical design criteria and investigating the extent to which the line parameters are modified with respect to the ideal case.

The effect of upper shielding basically amounts to a reduction of the line impedance. This is clearly seen in Fig. 5(a), where the constant Z_{01} curves are given in the plane a/b-h_1/b, the substrate thickness being set to $h/b = 1$. Although the minimum cover height needed to avoid significant impedance lowering depends on the line impedance itself, as a conservative estimate the cover height should be at least $h_1 = 4b$. For $h/b = 1$, $b \sim 300$ μm, this means that $h_1 \sim 1$ mm. In practice, coplanar lines for MMIC's have conductor widths as small as 50 μm, which means for a 50-Ω line, $b \sim 100$ μm; in this case, h_1 should be at least 300 μm, a condition which is easily satisfied. As expected, conductor-backed coplanar lines (CPW2) are slightly less sensitive to shielding than free-standing coplanar waveguides for the same characteristic impedance (Fig. 6(a)). However, also for this case, the design criterion

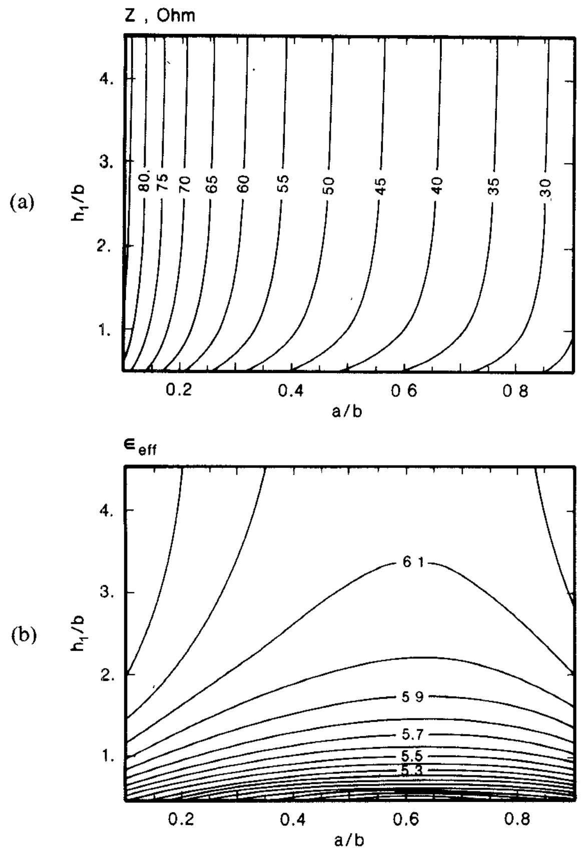

Fig. 5. (a) Constant-impedance and (b) effective permittivity curves for coplanar waveguide with upper shielding (CPW1) as a function of the shape ratio a/b and the cover height h_1/b with substrate thickness $h/b = 1$ and substrate permittivity $\epsilon_r = 13$.

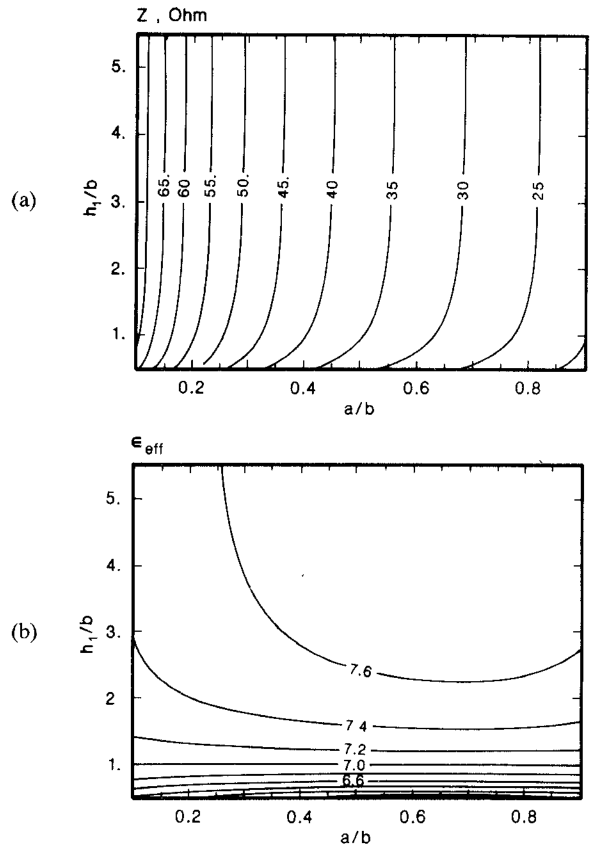

Fig. 6. (a) Constant-impedance and (b) effective permittivity curves for conductor-backed coplanar waveguide with upper shielding (CPW2) as a function of the shape ratio a/b and the cover height h_1/b with substrate thickness $h/b = 1$ and substrate permittivity $\epsilon_r = 13$.

$h_1 \geqslant 3b$ is a conservative estimate. In Figs. 5(b) and 6(b), the effective permittivities relative to the impedances of Figs. 5(a) and 6(a) are shown. A very different situation occurs when the shielding effect is given, mainly in hybrid or micro-hybrid circuits, by the flip-chip insertion of an active device on top of the coplanar line. The typical height of solder bumps, which sets the separation between the line and the metallized (grounded) surfaces lying on the active devices, is less than 50 μm; therefore, the local influence of flip-chip insertion on the line impedance is never negligible, unless lines with very small widths are used. This is customarily the case, owing to the need of connecting device pads of very small extent. A more complete discussion concerning the effect of flip-chip insertion can be found in [8] and [9].

Conductor backing lowers the impedance level of the line without heavily affecting the impedance behavior with respect to the parameter a/b. However, the amount of such impedance reduction greatly depends on the substrate thickness. If the dielectric layer is comparatively thin ($h/b = 1$), as in Fig. 6(a), impedance reduction can be 20 percent or more with respect to the free-standing structure. Therefore, conductor backing would allow the line to take on low impedance values independent of the ratio a/b. However, this can be a somewhat poor advantage, since the slot width $2b$ has to be increased in order to allow the upper ground plane to play a significant role, the substrate thickness being constant, thereby increasing circuit size. In fact, the usual trend in coplanar design tries to obtain the opposite result—making use of conductor backing to improve the mechanical properties of the circuit and power capabilities without heavily affecting the electrical behaviour in comparison with a free-standing CPW. In Fig. 7(a), a design chart for a conductor-backed CPW is presented giving the constant-impedance curves in the a/b-h/b plane with $h_1 \to \infty$ (upper cover removed); h/b varies between 1 and 5. For high h/b values, the impedance depends only on a/b. The minimum substrate thickness needed to make the line independent of h depends of course on the impedance itself, but a rough estimate for a 50-Ω line suggests $h/b > 3$ as a reasonable value (error with respect to $h/b \to \infty$ less than 2 percent, see Fig. 7(a)). From a practical point of view, this means, with $h = 300$ μm, $b = 100$ μm or less, and $a \sim 40$ μm or less for a $\sim$ 50-Ω line on GaAs, all acceptable values. Nevertheless, these can be limiting values for power applications, since decreasing the line width increases ohmic losses and power dissipation. Finally, in Fig. 7(b), the effective permittivities relative to the chart of Fig. 7(a) are shown.

Finite ground-plane width leads to a slight increase of the line impedance with respect to the ideal case ($c \to \infty$, or $b/c \to 0$). The amount of this effect is rather critical, since as is shown in the design chart of Fig. 8(a) ($h/b = 1$, c/b ranging from 1 to 3.33), for very narrow lateral

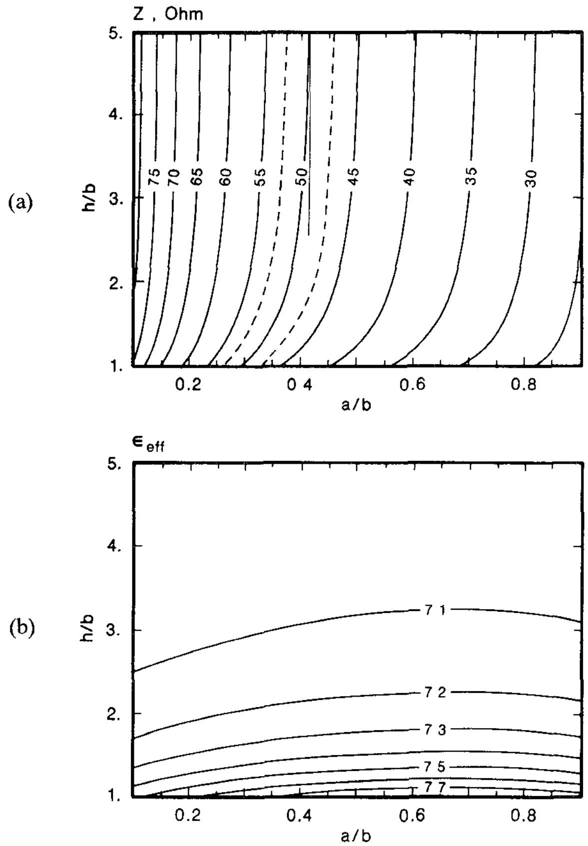

Fig. 7. (a) Constant-impedance and (b) effective permittivity curves for conductor-backed coplanar waveguide (CPW2) without upper shielding as a function of the shape ratio a/b and the substrate thickness h/b with substrate permittivity $\epsilon_r = 13$.

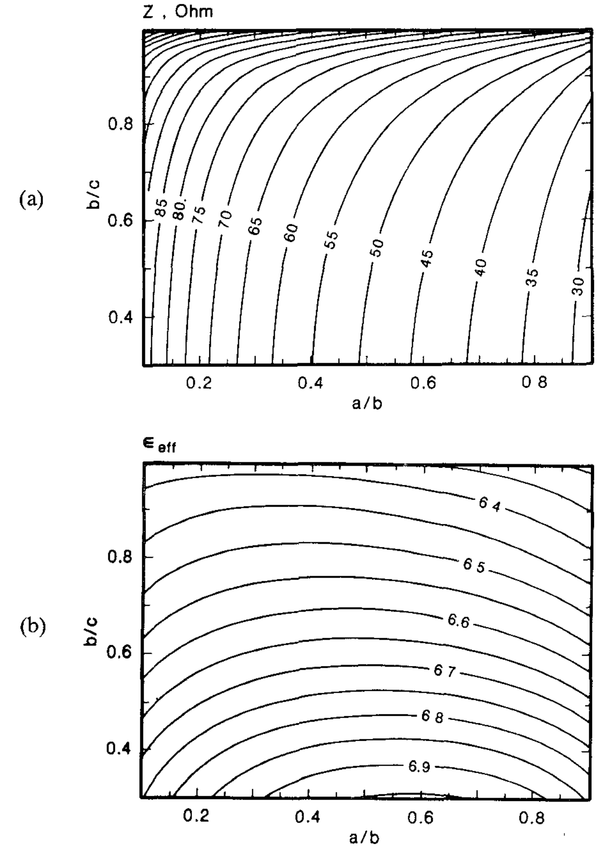

Fig. 8. (a) Constant-impedance and (b) effective permittivity curves for coplanar waveguide with finite ground planes, even mode (CPW3) as a function of the shape ratio a/b and the inverse of the ground plane width b/c with substrate thickness $h/b = 1$ and substrate permittivity $\epsilon_r = 13$.

ground planes, the impedance variation is dramatic. As a conservative estimate, one should have $c/b = 4$ at least to ensure that the variation is negligible. It should be noted that this problem is closely connected to line-to-line coupling, since lateral ground plane width also sets a lower limit on line spacing. As has been noted in [10], however, the impedance increases due to ground-plane truncation could be exploited in order to obtain high-impedance lines without excessively reducing the central conductor width. In Fig. 8(b), the effective permittivity relative to the impedance chart of Fig. 8(a) is shown.

Let us consider now the effect of the odd (parasitic) mode of a coplanar line with finite ground planes. As is clearly seen from Fig. 9, giving the constant odd-mode impedance curves in the a/b-b/c plane for infinitely thick substrate, the impedance level of the mode is high and anyway comparable to the one of the even mode. The dotted level curves represent the even-mode impedances. Therefore, proper grounding is mandatory in correspondence of launchers and discontinuities in order to avoid propagation of the parasitic mode. In particular, it is advisable to avoid transitions between CPW and two-conductor lines where only the center conductor and one lateral ground plane are connected, unless a grounding point is available nearby. However, such problems are of minor importance within MMIC's, since this kind of transition is rarely found there. A more serious problem concerns the possible presence of almost floating metallized regions due to poor grounding; the solution can be found either in proper circuit layout or, when conductor backing is introduced, in the usual via–hole or wraparound techniques.

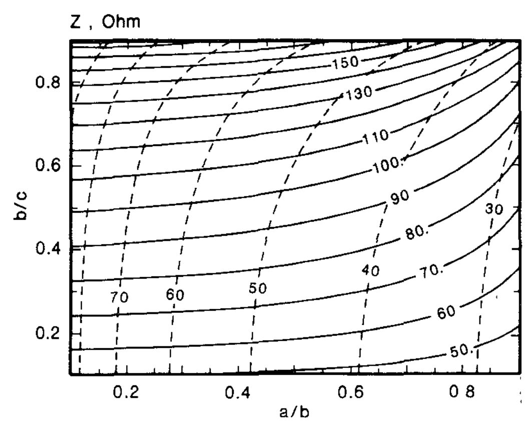

Fig. 9. Constant-impedance curves for coplanar waveguide with finite ground planes and infinitely thick substrate. Odd mode (CPW4) is denoted by continuous curves, even mode by dashed curves. The substrate permittivity is $\epsilon_r = 13$. For the definition of even- and odd-mode impedances, see text.

As a last point, let us consider line-to-line coupling (Fig. 1(d)). A chart for evaluating this effect, based on the

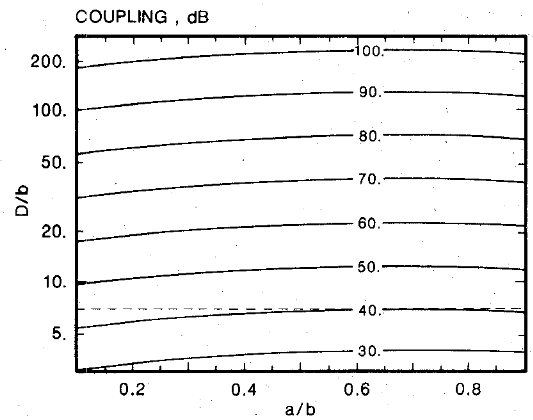

Fig. 10. Constant-coupling curves for parallel coplanar lines on infinitely thick GaAs substrate ($\epsilon_r = 13$) as a function of the shape ratio a/b and the normalized distance D/b (log scale).

analytical formulas previously discussed, is shown in Fig. 10, yielding constant-coupling curves in the plane a/b-D/b. It can be seen that coupling weakly depends on the shape ratio a/b, whereas, as is obvious, it is strongly influenced by the line spacing D. From Fig. 10, the minimum D needed to ensure coupling less than a given value can be obtained. As a conservative estimate of maximum coupling allowed, one can assume, for instance, the value of 40 dB, thereby requiring line spacing to be at least $D/b = 7$. For $D/b = 5$, the coupling is about 35 dB. It should be noted that such values are consistent with the limits obtained for lateral ground plane spacing, which are slightly lower than those imposed by the requirement on coupling.

IV. Conclusions

A number of parasitic effects occurring in the practical implementation of coplanar lines for MMIC applications have been discussed. Models and design formulas are proposed allowing for the presence of upper shielding, conductor backing, and finite-extent lateral ground planes. The effect of improper grounding on the excitation of a parasitic mode has been pointed out, and an approximate evaluation of line-to-line coupling has been proposed. Design criteria have been obtained for lines on GaAs substrates. Taking into account the parameter definitions in Fig. 1(a)–(d), one must have for the cover height $h_1 > 3b$, for the substrate height in conductor-backed lines $h > 3b$, and for the lateral ground plane width $c > 4b$ and $D > 7b$ in order for line-to-line coupling to be less than 40 dB. These criteria hold for coplanar lines on GaAs substrates.

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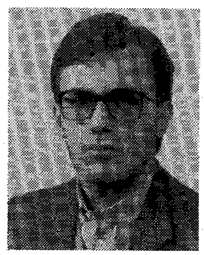

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